DIGITAL PROGRAMMABLE DELAY SCHEME WITH AUTOMATIC CALIBRATION

ABSTRACT

The digital programmable delay scheme with automatic calibration is an alternative to PLLs, DLLs, fixed delay cells and other methods of delay. The method and circuit sets a delay in a programmable delay cell in an oscillator circuit and uses a reference clock to calibrate the oscillator clock frequency. The programmable delay, once set, may then be used to determine a desired delay for a signal that passes through the programmable delay cell as well as another portion of the oscillator circuit. The circuit preferably uses two counters that are controlled by calibration and control logic in which one counter is clocked by the reference clock and the other is clocked by the oscillator circuit clock. After a predetermined time, the calibration and control logic compares the two count values and determines if the programmable delay cell of the oscillator circuit needs to be adjusted. If the oscillator circuit is determined to need adjustment, the calibration and control logic circuit so adjusts the programmable delay cell. The resulting circuit is small, flexible, and PVT calibrated and consumes very little power. It can be used with any reference clock to support various timing requirements at different frequencies.